Alpha Bridge AQSOH-T-A5-PBV Datasheet

Features

- Up to 800Gb/s data rate
- 8x100Gb/s PAM4 modulation
- Compatible to QSFP-DD Hardware Specification
- Compatible to IEEE802.3cK
- Hot-pluggable
- Power Supply Voltage: 3.3W
- RoHS compliant
- Operating temperature range: 0℃ to 70℃

Application

- Switches, Servers, Routers, Storage Arrays
- Networking Equipment
- Data Cables
- Telecommunications Central Offices
- Test and Measurement Equipment
- Test and Measurement Equipment

Description

AlphaBridge QSFP-DD800 (Double Density) Passive Direct Attach Copper Cable features 8 transmitting and 8 receiving 100Gbps PAM4 channels for 800G operation. The cable assembly meets IEEE 802.3ck 400GBase -CR4, 200Gbase-CR2, and 100GBase-CR1 standards with substantial signal integrity margin providing high performance and bandwidth interconnect solutions for high-density applications.

As next-gen data centers deploy faster speed in a tighter space, they need high-performance cables that reduce power consumption, provide reliable operation, and are low-cost. AlphaBridge QSFP-DD800 cable is designed to meet the next-gen data center needs. With unique foam dielectric construction, Volex QSFP-DD800 cable offers the smallestcable outer diameter and bend radius, and the highest flexibility, while meeting or exceeding the MSA signal integrity specification.

Absolute Maximum Ratings

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Storage Temperature	*TS*	-40		85	℃
Supply Voltage	*VCC3*	3.135		3.465	V
Relative Humidity (non-condensation)	*RS*	5		85	%

Recommended Operating Conditions & Power Supply Requirements

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Operating Case Temperature	*TOP*	0		70	℃
Power Supply Voltage	*VCC3*	3.135		3.465	V
Voltage on LVTTL Input	Vilvttl	-0.3		VCC3 +0.2	V

Power Supply Current	*Icc3*	0.001			mA

Frequency Domain

Item	*Test Parameter*	*IEEE802.3ck Specification*
1	Differential Insertion Loss (SDD21)	Maximum insertion loss at 26.56GHz -19.75dB Minimum insertion loss at 26.56GHz -11dB
2	Common Mode Reflection (SCC11/SCC22)	-1.4dB @ 0.05 to 6GHz -0.68-0.12*(f) @ 6 to 30GHz -10.28+0.2*(f) @ 30 to 40GHz
3	Common Mode Conversion (SCD11/SCD22)	-22+(10/25.56)*(f) @ 0.05 to 26.56GHz -15+(3/25.56)*(f) @ 26.56 to 40GHz
4	Differential to Common Mode Conversion Loss (SCD21-SDD21)	-10dB @ 0.05 to 12.89GHz -14+0.3108*(f) @ 12.89 to 40GHz
5	Channel Operating Margin (COM)	3dB Minimum
6	Effective Return Loss (ERL)	* 8.25 dB Minimum. Cable assemblies with a COM greater than 4 dB are notrequired to meet minimum ERL
7	Insertion Loss* (SDD21) for 0.5M 30awg	25.65GHz : -14.55 dB Max
	Insertion Loss* (SDD21) for 1.0M 28awg	25.65GHz : -16.75 dB Max
	Insertion Loss* (SDD21) for 1.5M 26awg	25.65GHz : -17.45 dB Max
	Insertion Loss* (SDD21) for 2.0M 26awg	25.65GHz : -19.75 dB Max

Pin Description

Pin#	Symbol	Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	Open-Drain with pull-up resistor on Host
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	

17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	See pin description for required circuit
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

Note:

LPWn/PRSn:

LPWn/PRSn is a dual-function signal that allows the host to signal Low Power mode and the module to indicate Module Present. The circuit shown in Figure 13-5 enables multi-level signaling to provide direct signal control in both directions. Low Power mode is an active-low signal on the host which gets converted to an active-low signalon the module. Module Present is controlled by a pull-down resistor on the module which gets converted to an active-low logic signal on the host.

31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	See the pin description for required circuit
45	VCC	+3.3V Power	Power from Host	2		
46	VCC	+3.3V Power	Power from Host	2		
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	Open-Drain with a pull-up resistor on the Host
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	

50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Note:

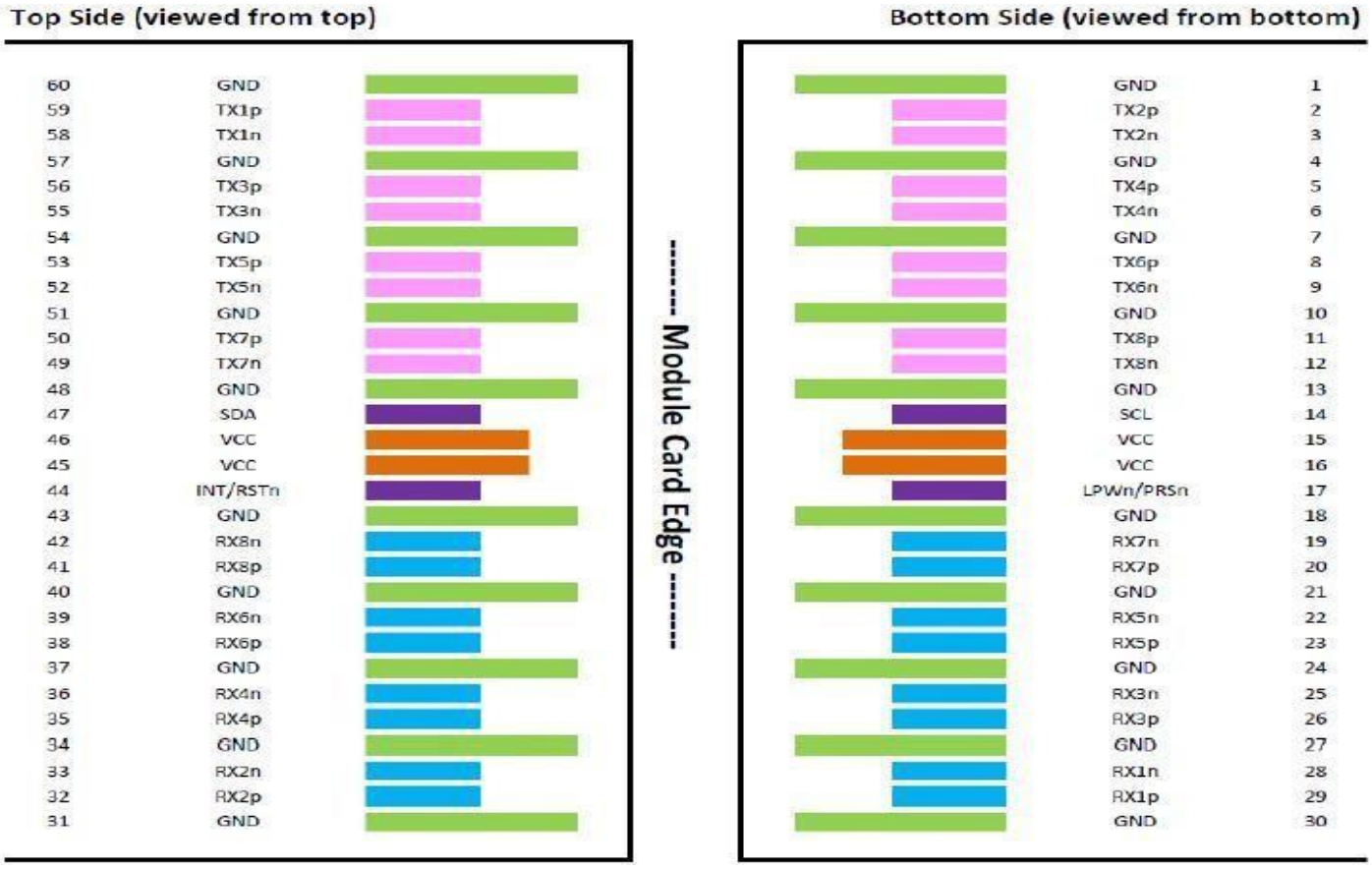
SDA and SCL:

SCL and SDA are a 2-wire serial interface between the host and module using the I2C or I3C protocols. SCL is defined as the serial interface clock signal and SDA as the serial interface data signal. Both signals are open -drain and require pull-up resistors to +3.3V on the host. The pull-up resistor value shall be 1k ohms to 4.7k ohms depending on capacitive load.

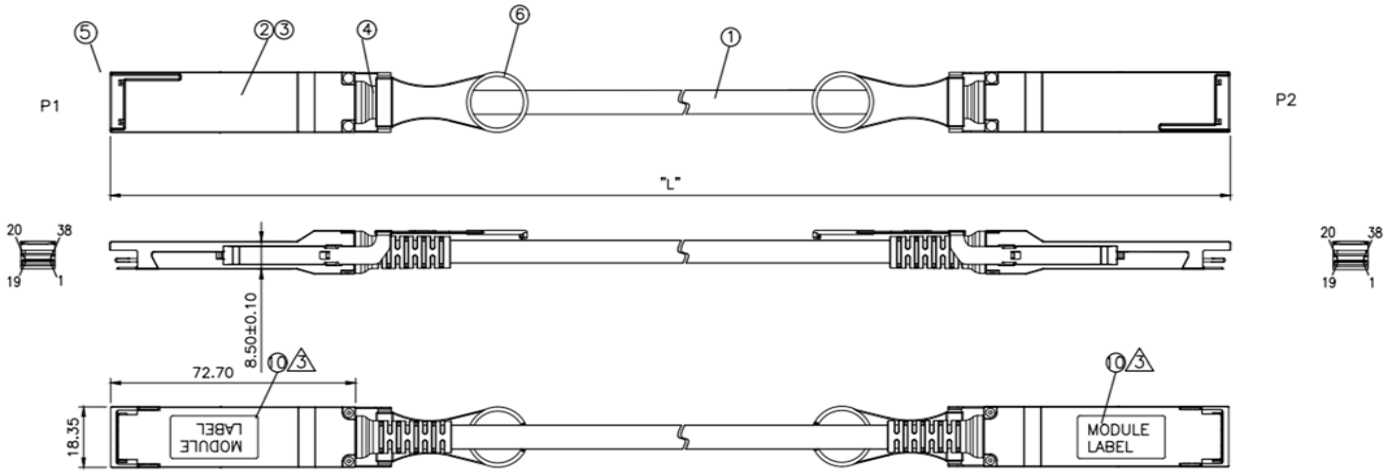
INT/RSTn:

INT/RSTn is a dual-function signal that allows the module to raise an interrupt to the host and also allows the host to reset the module. The circuit shown in Figure 13-3 enables multi-level signaling to provide direct signal control in both directions. Reset is an active-low signal on the host which is translated to an active-low signal on the module. An interrupt is an active-high signal on the module which gets translated to an active-high signal on the host

Pin Assignment



Dimensions



Ordering Information

Model Number	*Part Number*	*AWG*	*Length*	*Temperature*
800G OSFP DAC-1.5M	AQSOH-T-A5-PBV	26	1.5M	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.