Alpha Bridge AQSDH-T-X5-PEV Datasheet

Features

- Up to 800Gb/s data rate
- 8x100Gb/s PAM4 modulation
- Compatible to QSFP-DD Hardware Specification
- Compatible to IEEE802.3cK
- Hot-pluggable
- Power Supply Voltage: 3.3W
- RoHS compliant
- Operating temperature range: 0℃ to 70℃

Application

- Switches, Servers, RouterS, Storage Arrays
- Networking Equipment
- Data Cables
- Telecommunications Central Offices
- Test and Measurement Equipment
- Test and Measurement Equipment

Description

AlphaBridge QSFP-DD800 (Double Density) Passive Direct Attach Copper Cable features 8 transmitting and 8 receiving 100Gbps PAM4 channels for 800G operation. The cable assembly meets IEEE 802.3ck 400GBase -CR4, 200Gbase-CR2 and 100GBase-CR1 standards with substantial signal integrity margin providing high performance and bandwidth interconnect solutions for high-density applications.

As next-gen data centres deploy faster speed in a tighter space, they need high performance cables that reduce power consumption, provide reliable operation and are low cost. AlphaBridge QSFP-DD800 cable is designed to meet the next-gen data centre needs. With unique foam dielectric construction, Volex QSFP-DD800 cable offers smallestcable outer diameter and bend radius, and highest flexibility, while meeting or exceeding the MSA signal integrity specification.

Absolute Maximum Ratings

Parameter	*Symbol*	*Min.*	*Typ.*	*Max.*	*Units*
Storage Temperature	*TS*	-40		85	℃
Supply Voltage	*VCC3*	3.135		3.465	V
Relative Humidity (non-condensation)	*RS*	5		85	%

Recommended Operating Conditions & Power Supply Requirements

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Case Temperature	*TOP*	0		70	℃
Power Supply Voltage	*VCC3*	3.135		3.465	V
Voltage on LVTTL Input	Vilvttl	-0.3		VCC3 +0.2	V
Power Supply Current	*Icc3*	0.001			mA

Frequency Domain

Item	Test Parameter	IEEE802.3ck Specification
1	Differential Insertion Loss (SDD21)	Maximum insertion loss at 26.56GHz -17.16dB Minimum insertion loss at 26.56GHz -8dB
2	Common Mode Reflection (SCC11/SCC22)	-1.4dB @ 0.05 to 6GHz -0.68-0.12*(f) @ 6 to 30GHz -10.28+0.2*(f) @ 30 to 40GHz
3	Common Mode Conversion (SCD11/SCD22)	-22+(10/25.56)*(f) @ 0.05 to 26.56GHz -15+(3/25.56)*(f) @ 26.56 to 40GHz
4	Differential to Common Mode Conversion Loss (SCD21-SDD21)	-10dB @ 0.05 to 12.89GHz -14+0.3108*(f) @ 12.89 to 40GHz
5	Channel Operating Margin (COM)	3dB Minimum
6	Effective Return Loss (ERL)	* 8.25 dB Minimum. Cable assemblies with a COM greater than 4 dB are notrequired to meet minimum ERL
7	Insertion Loss* (SDD21) for 0.5M 30awg	25.65GHz : -14.55 dB Max
	Insertion Loss* (SDD21) for 1.0M 28awg	25.65GHz : -16.75 dB Max
	Insertion Loss* (SDD21) for 1.5M 26awg	25.65GHz : -17.45 dB Max
	Insertion Loss* (SDD21) for 2.0M 26awg	25.65GHz : -19.75 dB Max

Pin Description

Pin	Logic	Symbol	Description	Notes
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted DataInput	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted DataInput	
7		GND	Ground	1
8	LVTTL-I	ModSelL	Module Select	

9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	
11	LVCMOSI/O	SCL	2-wire serial interface clock	2
12	LVCMOSI/O	SDA	2-wire serial interface data	2
13		GND	Ground	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	2
28	LVTTL-O	IntL	Interrupt	2
29		Vcc Tx	+3.3V Power Supply transmitter	
30		Vcc1	+3.3V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data output	
42		GND	Ground	
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data output	
45		GND	Ground	
46	LVCMOS/CML-I	P/VS4	Programmable/Module Vendor Specific 4	
47	LVCMOS/CML-I	P/VS1	Programmable/Module Vendor Specific 1	

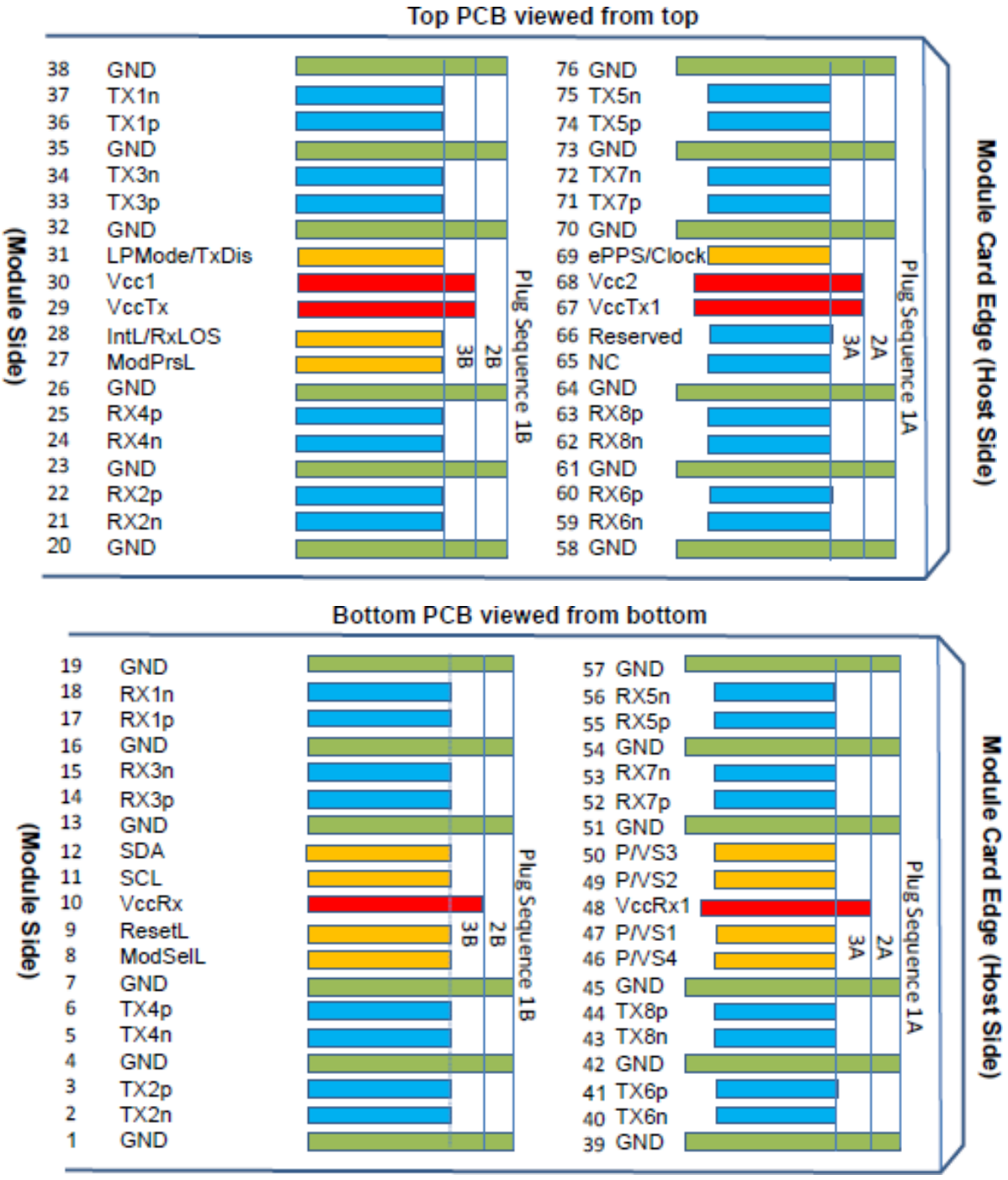
48		VccRx1	+ 3.3V Power Supply	
49	LVCMOS/CML-O	P/VS2	Programmable/Module Vendor Specific 2	
50	LVCMOS/CML-O	P/VS3	Programmable/Module Vendor Specific 3	
51		GND	Ground	
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	
58		GND	Ground	
59	CML-O	Rx6n	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	
65		NC	No Connect	
66		Reserved	For future use	
67		VccTx	+3.3 V Power Supply	
68		Vcc2	+3.3 V Power Supply	
69	LVCMOS-I	ePPS/Clock	1PPS PTP clock or reference clock input	
70		GND	Ground	
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Output	
73		GND	Ground	
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Output	
76		GND	Ground	

Note:

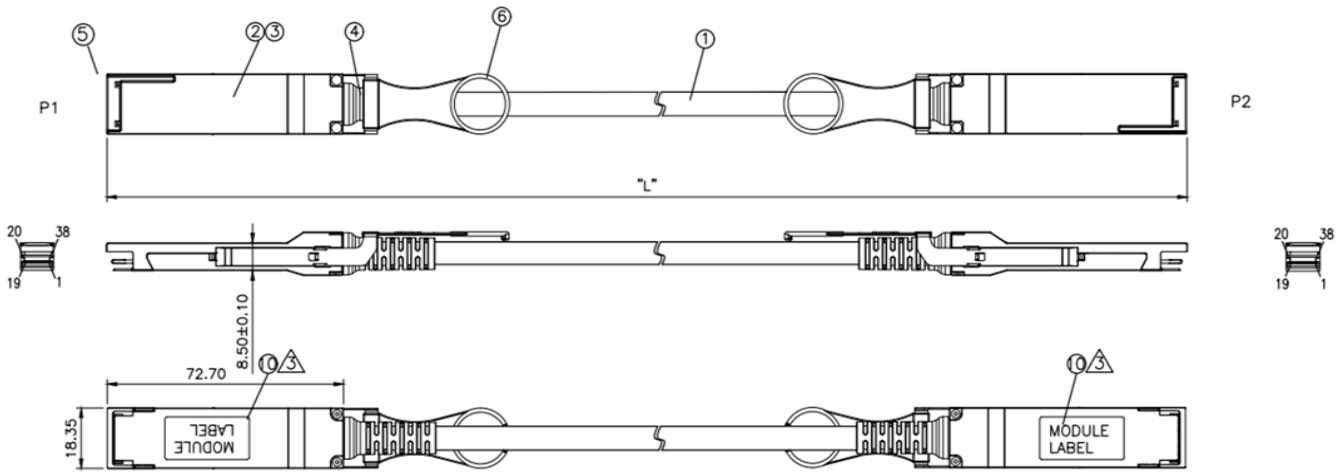
1. QSFP-DD 800G uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD 800G module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane. Each connector Gnd contact is ratedfor a maximum current of 500 mA.
2. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Supply requirements defined for the host side of the Host Card Edge Connector are listed in Table 10. For power classes 4 and above themodule differential loading of input voltage pads must not result in exceeding contact current limits. Each connector Vcc contact is rated for a maximum current of 1500 mA.
3. Reserved and no Connect pads recommended to be terminated with 10 k to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module.

4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD 800G pads. Sequence 1A and 1B will then occur simultaneously, followed by 2A and 2B,followed by 3A and 3B.
5. Full definitions of the P/VSx signals currently under development. On new designs not used P/VSx signals are recommended to be terminated on the host with 10 kΩ.
6. ePPS/Clock if not used recommended to be terminated with 50Ω to ground on the host

Pin Assignment



Dimensions



Ordering Information

Model Number	*Part Number*	*AWG*	*Length*	*Temperature*
800G QSF-DD DAC-0.5M	AQSDH-T-X5-PEV	30	0.5M	0 °C to 70 °C

Note: All information contained in this document is subject to change without notice.