Alpha Bridge AQSFP-DD-LR4 Datasheet

Features

- QSFP-DD MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- 100G Lambda MSA 400G-LR4 Specification compliant
- Up to 10km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0°C to 70°C
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel.
- Maximum power consumption 10.5W
- Duplex LC connector
- RoHS compliant

Applications

- Data Center Interconnect
- 400G Ethernet
- Infiniband interconnects
- Enterprise networking

Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 10km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 10km fiber transmission.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	*Ts*	-40	85	°C	
Operating Case Temperature	T_{op}	0	70	°C	
Power Supply Voltage	V_{cc}	-0.5	3.6	V	
Relative Humidity (non-condensation)	*RH*	0	85	%	
Damage Threshold, each Lane	*THd*	5		dBm	

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Operating Case Temperature	T_{op}	0		70	°C	
Power Supply Voltage	V_{cc}	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				$2.4x10^{-4}$		
Post-FEC Bit Error Ratio				$1x10^{-12}$		1
Link Distance	*D*	0.002		10	km	2

Notes:

1. FEC provided by host system.
2. FEC required on host system to support maximum distance.

Diagnostics Monitoring

Parameter	*Symbol*	*Accuracy*	*Unit*	*Notes*
Temperature monitor absolute error	DMI_Temp	± 3	℃	
Supply voltage monitor absolute error	DMI_VCC	± 0.1	V	
Channel RX power monitor absolute error	DMI_RX_Ch	± 2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	± 10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	± 2	dB	1

Notes:

1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Wavelength Assignment	*L0*	1264.5	1271	1277.5	nm	
	L1	1284.5	1291	1297.5		
	L2	1304.5	1311	1317.5		
	L3	1324.5	1331	1337.5		
Data Rate, each Lane		53.125 ± 100 ppm			GBd	
Modulation Format			PAM4			
Transmitter						
Side-mode Suppression Ratio	*SMSR*	30			dB	
Total Average Launch Power	P_T			11.1	dBm	
Average Launch Power, each Lane	*PAVG*	-2.7		5.1	dBm	1
Optical Modulation Amplitude (OMAouter), each Lane for TDECQ < 1.4dB for 1.4dB ≤ TDECQ ≤ 3.9dB	*POMA*	-0.3 -1.1+TDECQ		4.4	dBm	
Transmitter and Dispersion Eye Closure for PAM4, each Lane	*TDECQ*			3.9	dB	
TDECQ – TECQ|				2.5	dB	
Extinction Ratio	*ER*	3.5			dB	
Difference in Launch Power between any Two Lanes (OMA_{outer})				4	dB	
RIN17.1 OMA	*RIN*			-136	dB/Hz	
Optical Return Loss Tolerance	*TOL*			17.1	dB	
SMSR		*30*			dB	
Transmitter Reflectance	R_T			-26	dB	2
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	*Poff*			-16	dBm	
Receiver						
Damage Threshold, each Lane	*THd*	6.1			dBm	3
Average Receiver Power, each Lane		-9		5.1	dBm	4
Receiver Power (OMA_{outer}), each Lane				4.4	dBm	
Difference in Receiver Power between any Two Lanes (OMAouter)				4.3	dB	
Receiver Sensitivity (OMA_{outer}), each Lane for TECQ < 1.4dB for 1.4 dB ≤ TECQ ≤ 3.9 dB	*SEN*			-6.8 -8.2+ TECQ	dBm	
Stressed Receiver Sensitivity in OMAouter	*SRS*			-4.3	dBm	1
Receiver Reflectance	R_R			-26	dB	
LOS Assert	*LOSA*	-20			dBm	
LOS De-assert	*LOSD*			-2.1	dBm	
LOS Hysteresis	*LOSH*	0.5			dB	
Stressed Conditions for Stress Receiver Sensitivity (Note 7)						

Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.9		dB	
SECQ-10*$\log_{10}(C_{eq})$, Lane under Test					dB	
OMA_{outer} of each Aggressor Lane			-0.4		dBm	

Notes:

1. Average launch power, each lane (min) is informative and not the principal indicator of signal strength. A
2. transmitter with launch power below this value cannot be compliant, however, a value above this does not ensure compliance.
3. Transmitter reflectance is defined looking into the transmitter.
4. The receiver shall be able to tolerate, without damage, continuous exposure to an optical signal having this average power level. The receiver does not have to operate correctly at this input power.
5. Average receiver power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant, however, a value above this does not ensure compliance.
6. The receiver shall be able to tolerate, without damage, continuous exposure to an optical input signal having this average power level.
7. Measured with conformance test signal at TP3 (see 3.14) for the BER specified in IEEE Std 802.3-2018 clause 124.1.1.
8. These test conditions are for measuring stressed receiver sensitivity. They are not characteristics of the receiver.

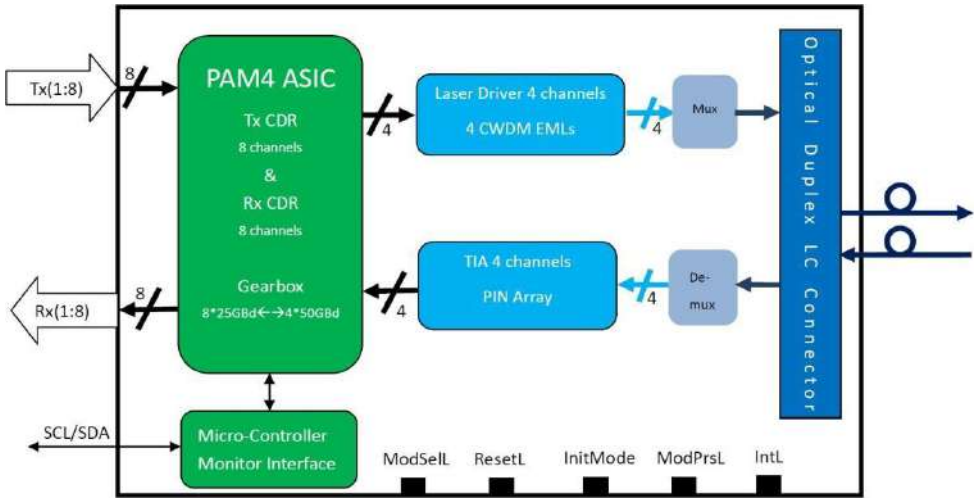
Electronical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Power Consumption				12	W	
Supply Current	*Icc*			3.64	A	
Signaling Rate, each Lane	*TP1*	26.5625 ± 100 ppm	GBd			
Transmitter (each Lane)						
Differential pk-pk input Voltage Tolerance	*TP1a*	900			mVpp	1
Differential Termination Mismatch	*TP1*			10	%	
Differential Input Return Loss	*TP1*	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	*TP1*	IEEE802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	*TP1a*	See IEEE 802.3bs 120E 3.4.1				2
Single-ended Voltage Tolerance Range (Min)	*TP1a*	-0.4 to 3.3			V	
DC Common Mode Input Voltage	*TP1*	-350		2850	mV	3
Receiver (each Lane)						
Differential Peak-to-Peak Output Voltage	*TP4*			900	mVpp	
AC Common Mode Output Voltage, RMS	*TP4*			17.5	mV	
Differential Termination Mismatch	*TP4*			10	%	
Differential Output Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-2)			mV	
Common to Differential Mode Conversion Return Loss	*TP4*	IEEE 802.3-2015 Equation (83E-3)				
Transition Time, 20% to 80%	*TP4*	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	*TP4*		-265		UI	
Near-end Eye Height, Differential	*TP4*	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	*TP4*		0.2		UI	
Far-end Eye Height, Differential	*TP4*	30			mV	
Far-end Pre-cursor ISI Ratio	*TP4*	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	*TP4*	-350		2850	mV	3

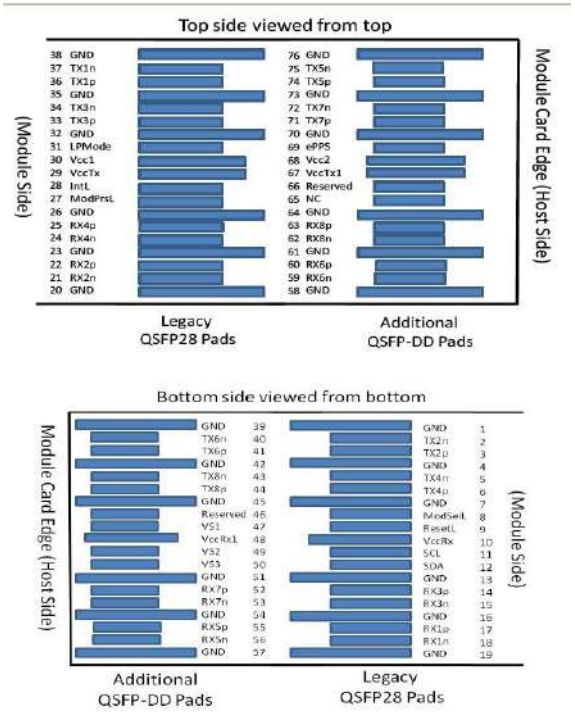
Notes:

1. With the exception to IEEE 802.3bs 120E.3.1.2 that the pattern is PRBS31Q or scrambled idle.
2. Meets BER specified in IEEE 802.3bs 120E 1.1
3. DC common mode voltage generated by the host. Specification includes effects of ground offset voltage.

Transceiver Block Diagram



Pin Assignment and Description



Pin Description

PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter inverted data input	
3	CML-I	Tx2p	Transmitter non-inverted data input	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted data input	
6	CML-I	Tx4p	Transmitter non-inverted data input	
7		GND	Ground	1
8	LVTTL-I	MoDSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		VccRx	+3.3v Receiver Power Supply	2
11	LVCMOS-I/O	SCL	2-wire Serial interface clock	
12	LVCMOS-I/O	SDA	2-wire Serial interface data	
13		GND	Ground	1

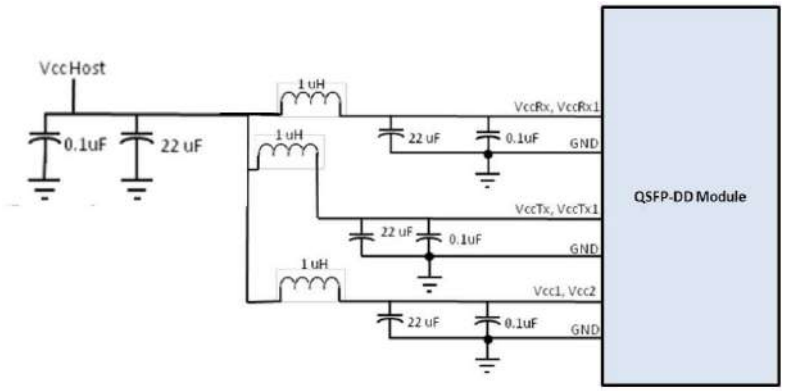
14	CML-O	RX3p	Receiver non-inverted Data Output	
15	CML-O	RX3n	Receiver inverted Data Output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver non-inverted Data Output	
18	CML-O	Rx1n	Receiver inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3v Power supply transmitter	2
30		Vcc1	+3.3v Power supply	2
31	LVTTL-I	LPMode	Low Power Mode	2
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	1
39		GND	Ground	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	
42		GND	Ground	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	
45		GND	Ground	1
46		Reserved	For future use	
47		VS1	Module Vendor Specific 1	
48		VccRx1	3.3V Power Supply	
49		VS2	Module Vendor Specific 2	
50		VS3	Module Vendor Specific 3	
51		GND	Ground	1
52	CML-O	Rx7p-	Receiver Non-Inverted Data Output	
53	CML-O	Rx7n	Receiver Inverted Data Output	
54		GND	Ground	1
55	CML-O	Rx5p-	Receiver Non-Inverted Data Output	
56	CML-O	Rx5n	Receiver Inverted Data Output	
57		GND	Ground	1
58		GND	Ground	1
59	CML-O	Rx6n-	Receiver Inverted Data Output	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	
61		GND	Ground	1
62	CML-O	Rx8n	Receiver Inverted Data Output	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	
64		GND	Ground	1
65		NC	No connect	3
66		Reserved	For future use	3
67		VccTx1	3.3V Power Supply	2
68		Vcc2	3.3V Power Supply	2

69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3
70		GND	Ground	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	
72	CML-I	Tx7n	Transmitter Inverted Data Input	
73		GND	Ground	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	
75	CML-I	Tx5n	Transmitter Inverted Data Input	
76		GND	Ground	1

Notes:

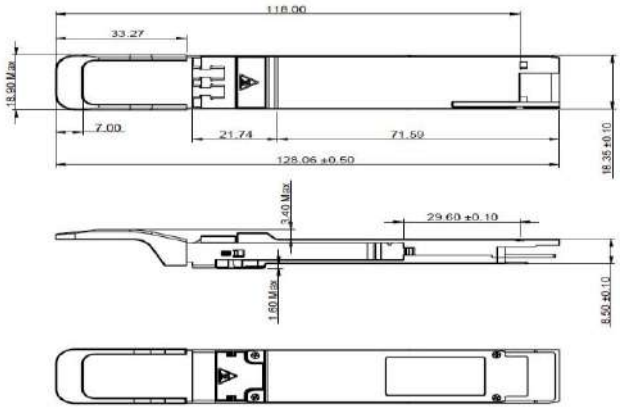
1. QSFP-DD uses common ground (GND) for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.
2. VccRx, RccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector. VccRx, VccRx1, Vccl, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The corrector Vcc pins are each rated for a maximum current of 1000mA.
3. All Vendor Specific, Reserved, No connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10k ohms and less than 100pF.
4. Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A, 1B will then occur simultaneously, followed by 2A, 2B, followed by 3A, 3B.

Recommended Power Supply Filter



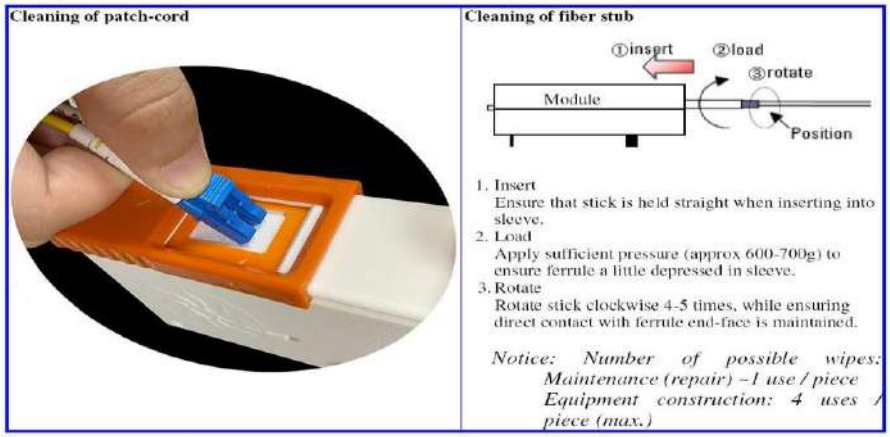
Host Board Power Supply Filtering

Dimensions



Optical Receptacle Cleaning Recommendations

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid.
Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.



Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

Model Number	Part Number	Voltage	Temperature
QSFP-DD-400G-LR4	OPDY-S10-13-CBE	3.3V	0°C to 70 °C