Alpha Bridge AQSFP28-100G-ER4 Datasheet

Descriptions

This module is designed for 40km optical communication applications. This module contains a 4-lane optical transmitter, a 4-lane optical receiver, and module management block including 2 wire serial interface. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector.

Features

- QSFP28 MSA-compliant
- Hot pluggable 38-pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- Transmitter: cooled LAN-WDM EMLTOSA
- Receiver: SOA+ PD ROSA
- Maximum power consumption 5W
- LC duplex connector
- Support 103.125Gb/s aggregate bit rate
- Up to 40km transmission on single-mode fiber with FEC
- Operating case temperature:0°C to 70°C
- Single 3.3V power supply
- RoHS 2.0 compliant

Application

- 100GBASE-ER4 100G Ethernet
- Telecom networking
- Data Center Interconnect.

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	Ts	-40	85	°C	
Max Supply Voltage	Vcc	0	3.6	V	
Relative Humidity	RH	15	85	%	1
Damage Threshold, each Lane	THd	5.5		dBm	

Note: Non-condensing

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Typ.
Case operating Temperature	Top	0	70	°C	
Supply Voltage	Vcc	3.135	3.465	V	3.3
Link distance with G.652			40	KM	

Transmitter Electro-optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Transmit wavelengths		1294.53		1296.59	nm	
		1299.02		1301.09	nm	
		1303.54		1305.63	nm	
		1308.09		1310.19	nm	
Signaling Speed per Lane	25.78125± 100 ppm				Gb/s	
Side-mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power				8.9	dBm	
Average launch power, each Lane		-2.9		2.9	dBm	
Optical Modulation Amplitude (OMA), each lane		0.1		4.5	dBm	
Difference in Launch Power between any Two Lanes (Averageand OMA)				3.6	dB	
Transmitter and Dispersion Penalty (TDP), each lane				2.5	dB	
Extinction Ratio	ER	8			dB	
RIN OMA				-130	dB/Hz	
Optical Return Loss Tolerance				20	dB	
Transmitter Reflectance				-12	dB	
Mask margin		5			%	
Transmitter eye mask definition {X1, X2,X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					1

Receiver Electro-optical Characteristics

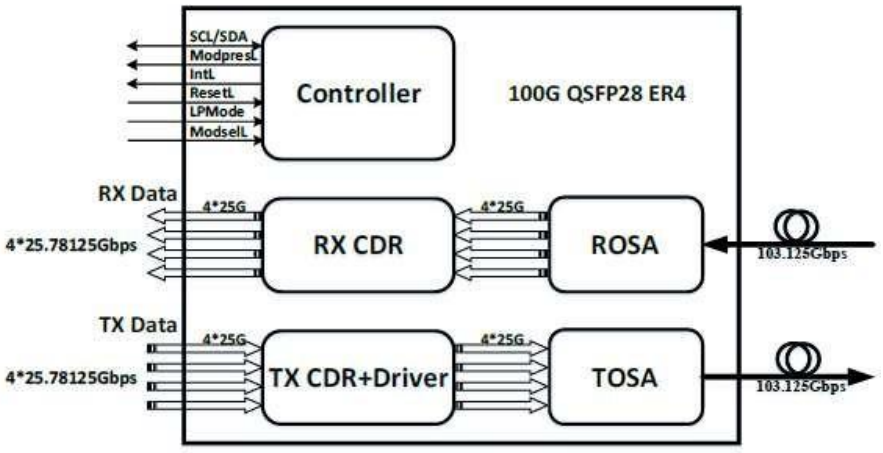
Parameter	Symbol	Min.	Typ.	Max.	Units	Note
		1294.53		1296.59	nm	
Receive wavelength		1299.02		1301.09	nm	
		1303.54		1305.63	nm	
		1308.09		1310.19	nm	
Signaling Speed per Lane	25.78125 ± 100 ppm				Gb/s	
Average Receiver Power, each Lane		-20.9		-3.5	dBm	
Receiver power, each lane (OMA)				-3.5	dBm	
Receiver reflectance				-26	dB	
Difference in receive power between any two lanes (Average and OMA)				4.5		
Receiver sensitivity (AOP), each lane				-20.9	dBm	2
Receiver 3 dB electrical upper cutoff frequency, each lane				31	GHz	
Damage Threshold, each Lane	THd	5.5			dBm	
LOS Assert	LOSA	-33			dBm	
LOS Deassert	LOSD			-22	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Notes:

1. Hit ratio 5 × 10−5.

2. Sensitivity is specified at BER@5E-5 with FEC

Block Diagram of Transceiver



ModSelL:

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communica- tion commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the Mod- SelL de-asserttime after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

ResetL :

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the mini- mum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) thehost shall disregard all status bits until the module indi-cates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset

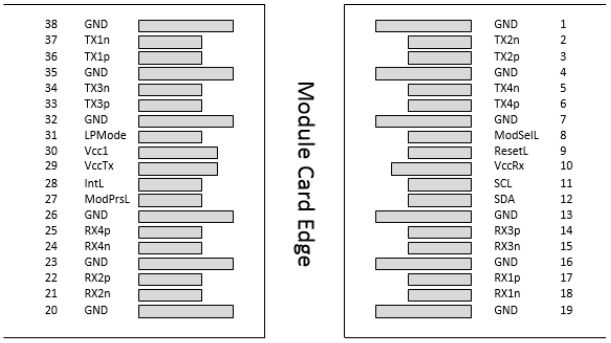
ModPrsL:

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when insertedand deasserted "High" when the module is physically absent from the host connector.

IntL:

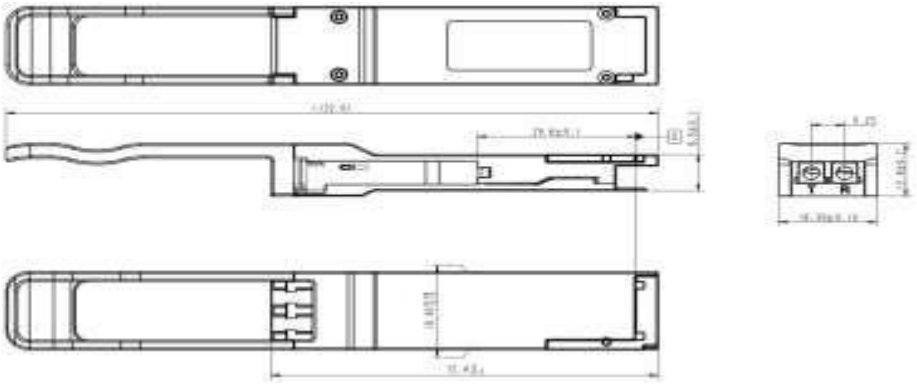
IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deas- serted "High" after completion of reset, when byte 2 bit0 (Data Not Ready) is read with a value of '0' and the flag field is read.

Pin Assignment (MSA compliant connector)



MSA compliant Connector

Dimensions



Note: Dimensions are in mm, All Dimensions are 0.2mm unless otherwise specified

Pin Descriptions

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Non-Inverted Data Output	
25	Rx4p	Receiver Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Lower Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Ordering information:

Model Number	Part Number	Voltage	Temperature
AQSFP28-100G-ER4	OPCW-S80-13-CR	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.

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