Alpha Bridge AQSFP-40G-SR4 Datasheet

Features

- 4 independent full-duplex channels
- Up to 11.2Gb/s data rate per channel
- MTP/MPO optical connector
- QSFP+ MSA compliant
- Digital diagnostic capabilities
- Up to 100m transmission on OM3 multi-mode ribbon fiber
- CML compatible electrical I/O
- Single +3.3V power supply
- Operating case temperature: 0 to 70oC
- XLPPI electric interface
- Maximum power consumption 1.5W
- RoHS-6 compliant

Applications

- Rack to Rack
- Data Center
- Infiniband QDR, DDR and SDR
- 40G Ethernet

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Storage Temperature	Ts	-40	85	℃
Supply Voltage	V_{cc}	-0.5	3.6	V
Operating Case Temperature	T_{opc}	0	70	℃
Relative Humidity (non-condensation)	RH	0	85	%
Damage Threshold, each Lane	THd	3.4		dBm

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating Temperature	Topc	0		70	℃
Power Supply Voltage	V_{cc}	3.1	3.3	3.465	V
Data Rate, each Lane			10.3125	11.2	Gb/s
Control Input Voltage High		2		Vcc	V
Control Input Voltage Low		0		0.8	V
Link Distance (OM3)	D			100	m

Diagnostics

Parameter	Symbol	Accuracy	Units	Notes
Temperature monitor absolute error	DMI_Temp	±3	℃	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	±0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	±2	dB 1	
Channel Bias current monitor	DMI_Ibias_Ch	±10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	±2	dB 1	

Notes: 1. Due to measurement accuracy of different single mode fibers, there could be an additional +/-1 dB fluctuation, or a +/- 3 dB total accuracy.

Transmitter Electro-optical Characteristics

Parameter	Symbol	Min	Type	Max	Units	Notes
Power Consumption				1.5	W	
Supply Current	ICC			450	mA	
Transceiver Power-on Initialization Time				2000	ms	1
Single-ended Input Voltage Tolerance (note 2)		-0.3		4	V	Referred to TP1 signal common
AC Common Mode Input Voltage Tolerance		15			mV	RMS
Differential Input Voltage Swing Threshold		50			mVpp	LOSA Threshold
Differential Input Voltage Swing	Vin,pp	180		1200	mVpp	
Differential Input Impedance	Zin	90	100	110	Ohm	
Differential Input Return Loss	See IEEE 802.3ba86A.4.11				dB	10MHz-11.1GHz
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage (DDPWS) Tolerance	0.07				UI	
Eye Mask Coordinates {X1,X2, Y1, Y2}	0.11, 0.31,95,350				UI v	Hit Ratio =5x10-5
Center Wavelength	λc	840	850	860	nm	
RMS Spectral Width	△λrms		0.5	0.65	Nm	
Average Launch Power, each Lane	PAVG	-7.6		1	dBm	3
Optical Modulation Amplitude (OMA), each Lane	POMA	-5.6		3	dBm	4
Difference in Launch Power between any Two Lanes (OMA)	Ptx,diff			4	dB	
Peak Power, each Lane	PPT			4	dBm	
Launch Power in OMA minusLaunch Power in OMA minus Transmitter and Dispersion Penalty (TDP), each Lane		-6.5			dBm	
TDP, each Lane				3.5	dB	
Extinction Ratio	ER	3			dB	
Relative Intensity Noise	RIN			-128	dB/Hz	12dB reflection
Optical Return Loss Tolerance	TOL			12	dB	
Encircled Flux	≥ 86% at 19um, ≤ 30% at 4.5um					
Transmitter Eye Mask Definition {X1, X2, X3, Y1, Y2, Y3}	0.23, 0.34, 0.43, 0.27, 0.35, 0.4					
Average Launch Power OFF Transmitter, each Lane	Poff			-30	dBm	

Notes:

1. Power-on Initialization Time is the time from when the power supply voltages reach and remain above theminimum recommended operating supply voltages to the time when the module is fully functional.
2. The single ended input voltage tolerance is the allowable range of the instantaneous input signals.
3. The maximum transmitter average optical power of 1.0 dBm is well within the guard band of receiver overload specifications of commercially available 10GBASE-SR SFP+ transceivers.
4. Even if the TDP < 0.9 dB, the OMA min must exceed the minimum value specified here.

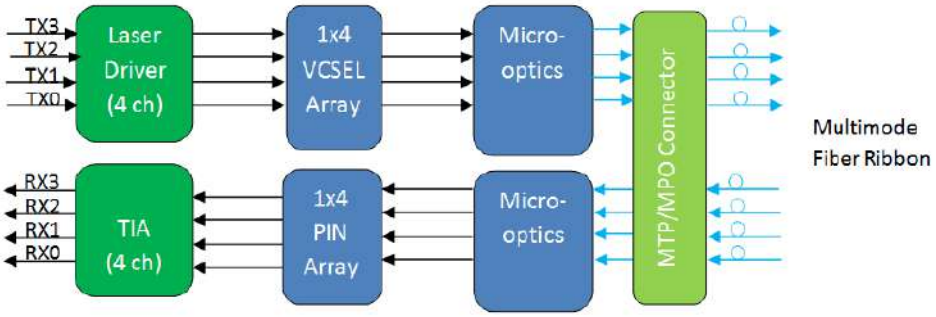
Electro Characteristics

Parameter	Symbol	Min	Type	Max	Units	Notes
Single-ended Output Voltage		-0.3		4	V	Referred to signal common
AC Common Mode Output Voltage				7.5	mV	RMS
Differential Output Voltage Swing	Vout,pp	600		800	mVpp	
Differential Output Impedance	Zout	90	100	110	Ohm	
Termination Mismatch at 1MHz				5	%	
Differential Output Return Loss	See IEEE 802.3ba 86A.4.2.1				dB	10MHz-11.1GHz
Common Mode Output Return Loss	See IEEE 802.3ba 86A.4.2.2				dB	10MHz-11.1GHz
Output Transition Time		28			ps	20% to 80%
J2 Jitter Output	Jo2			0.42	UI	
J9 Jitter Output	Jo9			0.65	UI	
Eye Mask Coordinates {X1, X2, Y1, Y2}	0.29, 0.5 , 150, 425				UI mV	Hit Ratio =5x10-5
Center Wavelength	Λc	840	850	860	nm	
Damage Threshold, each Lane	THd	3.4			dBm	1
Average Receive Power, each Lane		-9.5		2.4	dBm	
Receiver Reflectance	R_R			-12	dB	
Receive Power (OMA), each Lane				3	dBm	
Receiver Sensitivity (OMA), each Lane	SEN			-8.4	dBm	
Stressed Receiver Sensitivity (OMA), each Lane				5.4	dBm	2
Peak Power, each Lane	PP_R			4	dBm	
LOS Assert	LOSA	-30			dBm	
LOS Deassert	LOSD			-12	dBm	
LOS Hysteresis	LOSH	0.5			dB	
Vertical Eye Closure Penalty, each Lane			1.9		dB	
Stressed Eye J2 Jitter, each Lane			0.3		UI	
Stressed Eye J9 Jitter, each Lane			0.47		UI	
OMA of each aggressor lane			0.4		dBm	

Notes:

1. The receiver shall be able to tolerate, without damage, continuous exposure to a modulated optical inputsignal having this power level on one lane. The receiver does not have to operate correctly at this input power.
2. Measured with conformance test signal at receiver input for BER = $1x10^{-12}$.
3. Vertical eye closure penalty and stressed eye jitter are test conditions for measuring stressed receiversensitivity. They are not characteristics of the receiver.

Block Diagram of Transceiver



The OPCS-MX1-85-CB converts parallel electrical input signals into parallel optical signals, by a driven Vertical Cavity Surface Emitting Laser (VCSEL) array. The transmitter module accepts electrical input signals compatible with Common Mode Logic (CML) levels. All input data signals are differential and internally terminated. The receiver module converts parallel optical input signals via a photo detector array into parallel electrical output signals. The receiver module outputs electrical signals are also voltage compatible with Common Mode Logic (CML) levels. Alldata signals are differential and support a data rates up to 10 Gbps per channel. Figure 1 shows the functional block diagram of the OPCS-MX1-85-CB QSFP Transceiver.

A single +3.3V power supply is required to power up the module. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications the module offers 7 low speedhardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL andIntL.

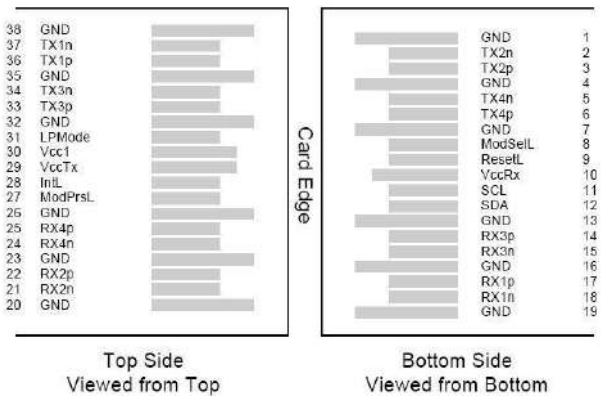
Module Select (ModSelL) is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP modules on a single 2-wire interface bus – individual ModSelL lines for each QSFP module must be used.
Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enablethe host to access the QSFP memory map.

The ResetL pin enables a complete module reset, returning module settings to their default state, when a low levelon the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up(including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

Low Power Mode (LPMode) pin is used to set the maximum power consumption for the module in order to protecthosts that are not capable of cooling higher power modules, should such modules be accidentally inserted.
Module Present (ModPrsL) is a signal local to the host board which, in the absence of a module, is normally pulledup to the host Vcc. When a module is inserted into the connector, it completes the path to ground though a resistoron the host board and asserts the signal. ModPrsL then indicates a module is present by setting ModPrsL to a “Low” state.

Interrupt (IntL) is an output pin. When “Low”, it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Pin Assignment



Pin Description

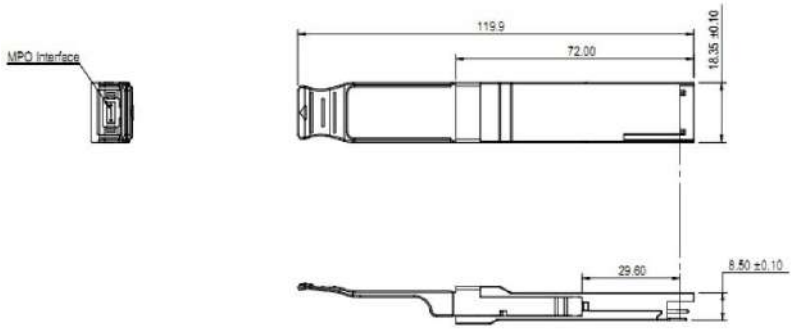
PIN	Logic	Symbol	Name/Description	Note
1		GND	Ground	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	
4		GND	Ground	1
5	CML-I	Tx4n	Transmitter inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	
7		GND	Ground	1
8	LVTLL-I	ModSeIL	Module Select	
9	LVTLL-I	ResetL	Module Reset	
10		VccRx	+3.3V Power Supply Receiver	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	
13		GNC	Ground	
14	CML-O	Rx3p	Receiver Non-Inverted Data output	
15	CML-O	Rx3n	Receiver Inverted Data output	
16		GND	Ground	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	1
20		GND	Ground	1
21	CML-O	Rx2n	Receiver Inverted Data output	
22	CML-O	Rx2p	Receiver Non-Inverted Data output	
23		GND	Ground	1
24	CML-O	Rx4n	Receiver Inverted Data output	
25	CML-O	Rx4p	Receiver Non-Inverted Data output	
26		GND	Ground	1
27	LVTTL-O	ModPrsL	Module Present	
28	LVTTL-O	IntL	Interrupt	
29		VccTx	+3.3V Power Supply transmitter	
30		Vcc1	+3.3V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Output	
35		GND	Ground	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Output	
38		GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for QSFP+ modules. All are common within the QSFP+ module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.

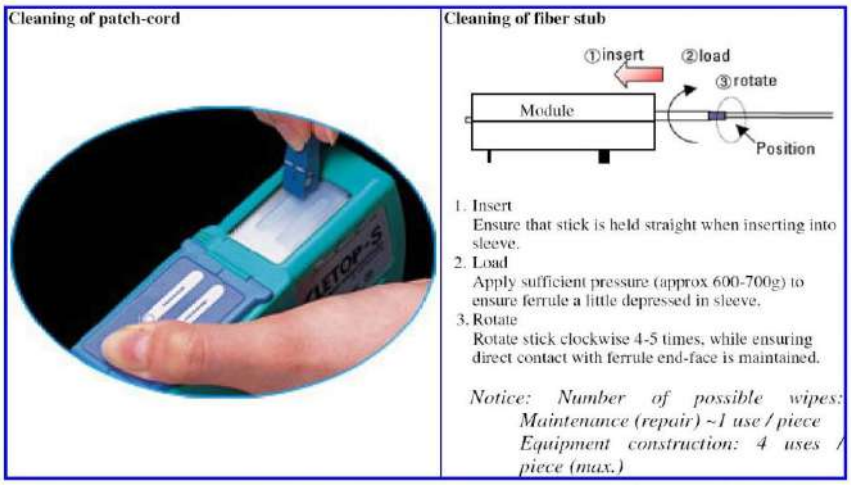
2. VccRx, Vcc1 and VccTx are the receiver and transmitter power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 4 below. Vcc Rx, Vcc1 and Vcc Tx maybe internally connected within the QSFP+ transceiver module in any combination. The connector pins are each rated for a maximum current of 500mA.

Dimensions



Optical Receptacle Cleaning Recommendations:

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop® stick type and HFE7100 cleaning fluid. Before the mating of patch- cord, the fiber end should be cleaned up by using Cletop® cleaning cassette.



Note: The pictures were extracted from NTT-ME website. And the Cletop® is a trademark registered by NTT-ME

Ordering Information

Model Number	Part Number	Voltage	Temperature
AQSFP-40G-SR4	OPCS-MX1-85-CB	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.