

# Alpha Bridge

## AQSFP28-100G-ZR4

### Datasheet

## Descriptions

This is designed for 80km optical communication applications. This module contains a 4-lane optical transmitter, 4-lane optical receiver, and module management block including 2 wire serial interface. The optical signals are multiplexed to a single-mode fiber through an industry standard LC connector.



## Features

- QSFP28 MSA-compliant
- Hot pluggable 38-pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- Maximum power consumption 5.5W
- LC duplex connector
- Supports 103.125Gb/s aggregate bit rate.
- Up to 80km transmission on single-mode fiber
- Operating case temperature:0°C to 70°C
- Single 3.3V power supply
- RoHS 2.0 compliant

## Application

- 100GBASE-ZR4 100G Ethernet
- Telecom networking

## Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	$T_s$	-40	85	°C	
Power Supply Voltage	$V_{CC}$	0	3.6	V	
Relative Humidity (non-condensation)	$RH$	15	85	%	1
Damage Threshold, each Lane	$TH_d$	6.5		dBm	

## Recommended Operating Conditions

Performance Item	Related Bytes(A0[00] memory)	Monitor Error	Notes
Module temperature	22 to 23	+/-3°C	1,2
Module voltage	26 to 27	< 3%	2
LD Bias current	42 to 49	< 10%	2
Transmitter optical power	50 to 57	< 3dB	2
Receiver optical power	34 to 41	< 3dB	2

**Transmitter Electro-optical Characteristics**

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Power Consumption				6.5	W	
Supply Current	<i>I<sub>cc</sub></i>			1.8759	A	Steady-state
Data Rate, each lane			25.78125		Gbps	
Differential Voltage pk-pk	<i>V<sub>pp</sub></i>			900	mV	At 1MHz
Common Mode Voltage	<i>V<sub>cm</sub></i>	-350		2850	mV	
Transition time	<i>T<sub>rise</sub>/T<sub>fall</sub></i>	10			ps	20%~80%
Differential Termination Resistance Mismatch				10	%	
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
Signaling Speed per Lane		25.78125 ± 100 ppm			Gb/s	
Transmit Wavelength		1294.53		129.59	nm	
		1299.02		1301.09	nm	
		1303.54		1305.63	nm	
		1308.09		1310.19	nm	
Side-Mode Suppression Ratio	<i>SMSR</i>	30			dB	
Total Average Launch Power	<i>P<sub>T</sub></i>	8		12.5	dBm	
Average Launch Power, each Lane	<i>P<sub>AVG</sub></i>	2		6.5	dBm	
Extinction Ratio	<i>ER</i>	6			dB	
Difference in Launch Power between any Two Lanes (Average and OMA)	<i>P<sub>tx,diff</sub></i>			3	dBm	
Average launch power of OFF transmitter, each lane	<i>P<sub>off</sub></i>			-30	dBm	
RIN <sub>20OMA</sub>	<i>RIN</i>			-130	dB/Hz	
Optical Return Loss Tolerance	<i>TOL</i>			20	dB	
Transmitter Reflectance	<i>R<sub>T</sub></i>			-12	dB	
Mask margin		5			%	
Eye Mask {X1, X2, X3, Y1, Y2, Y3}		{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}				1

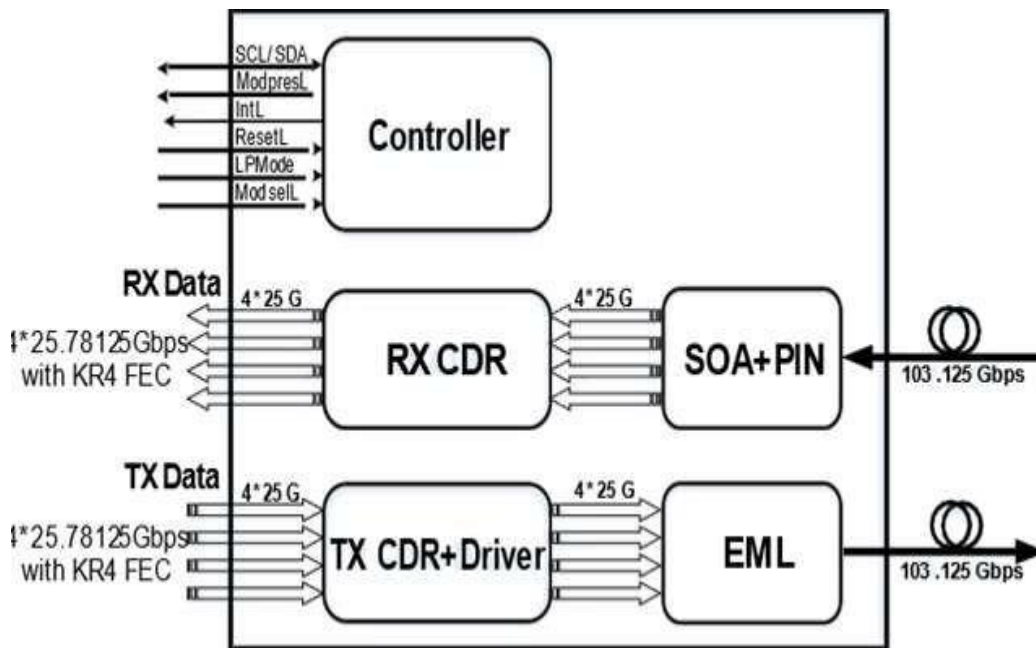
**Receiver Electro-optical Characteristics**

Parameter	Symbol	Min	Typ.	Max	Unit	Notes
Data Rate, each lane			25.78125		Gbps	
Differential Termination Resistance Mismatch				10	%	At 1 MHz
Differential output voltage swing	<i>V<sub>out, pp</sub></i>			900	mV	
Common Mode Noise, RMS	<i>V<sub>rms</sub></i>			17.5	mV	

Transition time	Trise/Tfall	12			ps	20%~80%
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	
Signaling Speed per Lane			25.78125		Gbps	
Receive Wavelength		1294.53		1296.59	nm	
		1299.02		1301.09	nm	
		1303.54	1305.63	1305.63	nm	
		1308.09	1310.19	1310.19	nm	
Average Receive Power, each Lane		-28	-3.5	-3.5	dBm	
Receive Power (OMA), each Lane				-3.5	dBm	
Receiver reflectance				-26	dB	
Receiver Sensitivity Average, each Lane				-28	dBm	1
Receiver 3 dB electrical upper cutoff frequency each lane				31	GHz	
				31	GHz	
Damage Threshold, each Lane	$TH_d$	6.5			dBm	
LOS Assert	LOSA	-40			dBm	
LOS Deassert	LOSD			-29	dBm	
LOS Hysteresis	LOSH	0.5			dBm	

Notes: Sensitivity is specified at BER@5E-5 with FEC

### Block Diagram of Transceiver



**ModSelL:**

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module.

In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

**ResetL :**

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length ( $t_{Reset\_init}$ ) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time ( $t_{init}$ ) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset ( $t_{init}$ ) the host shall disregard all status bits until the module indicates a completion of the reset interrupt.

The module indicates this by asserting "low" an IntL signal with the Data\_Not\_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset

**LPMODE:**

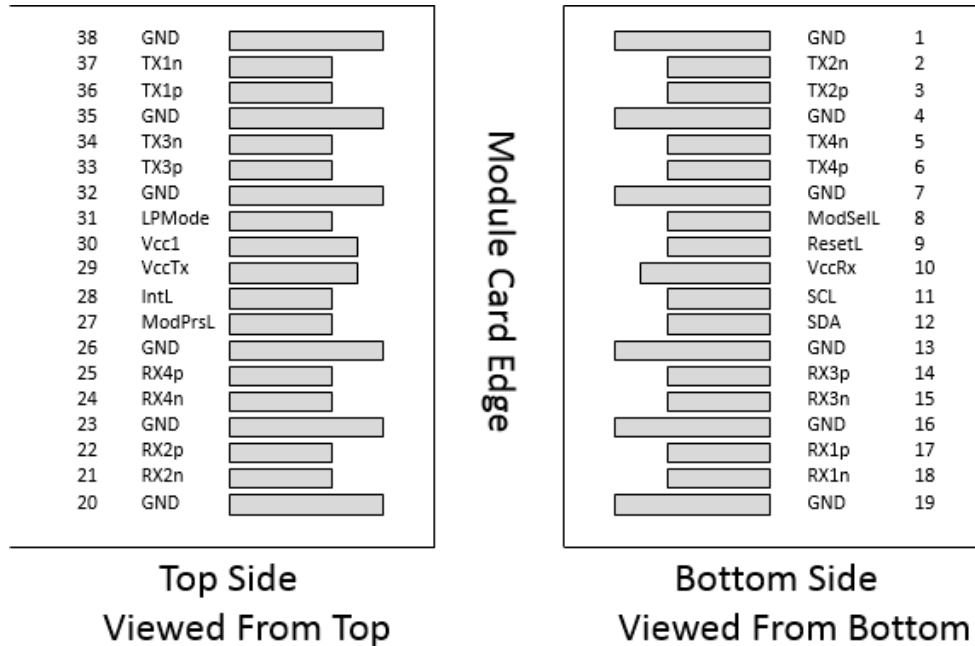
The LPMODE pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMODE pin and a combination of the Power override, Power\_set and High\_Power\_Class\_Enable software control bits (Address A0h, byte 93 bits 0,1,2).

**ModPrsL:**

ModPrsL is pulled up to Vcc\_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

**IntL:**

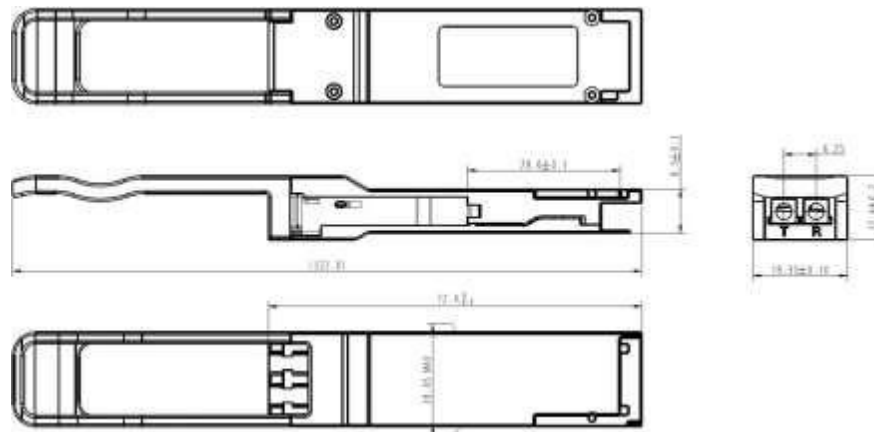
IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.

**Pin Assignment (MSA compliant connector)**

**Pin Descriptions**

Pin	Symbol	Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	

18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Non-Inverted Data Output	
25	Rx4p	Receiver Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMODE	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

### Dimensions


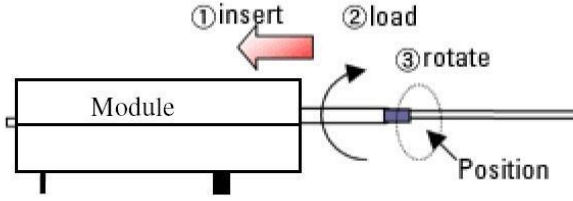


Note: Dimensions are in mm, All Dimensions are 0.2mm unless otherwise specified

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**Optical Receptacle Cleaning Recommendations :**

All fiber stubs inside the receptacle portions were cleaned before shipment. In the event of contamination of the optical ports, the recommended cleaning process is the use of forced nitrogen. If contamination is thought to have remained, the optical ports can be cleaned using a NTT international Cletop<sup>®</sup> stick type and HFE7100 cleaning fluid. Before the mating of patch-cord, the fiber end should be cleaned up by using Cletop<sup>®</sup> cleaning cassette.

<p><b>Cleaning of patch-cord</b></p> 	<p><b>Cleaning of fiber stub</b></p>  <ol style="list-style-type: none"> <li>1. Insert Ensure that stick is held straight when inserting into sleeve.</li> <li>2. Load Apply sufficient pressure (approx 600-700g) to ensure ferrule a little depressed in sleeve.</li> <li>3. Rotate Rotate stick clockwise 4-5 times, while ensuring direct contact with ferrule end-face is maintained.</li> </ol> <p><i>Notice: Number of possible wipes: Maintenance (repair) ~1 use / piece Equipment construction: 4 uses / piece (max.)</i></p>
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Note: The pictures were extracted from NTT-ME website. And the Cletop<sup>®</sup> is a trademark registered by NTT-ME

**Ordering information:**

Model Number	Part Number	Voltage	Temperature
AQSFP28-100G-ZR4	OPCW-S40-13-CR	3.3V	0°C to 70 °C

**Note: All information contained in this document is subject to change without notice.**