Alpha Bridge AQSFP28-100G-LR4 Datasheet

Alpha Bridge Technologies Pvt. Ltd.
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Features

- QSFP28 MSA compliant
- Compliant to IEEE 802.3ba 100GBASE-LR4
- Digital diagnostic monitoring support
- Hot pluggable 38 pin electrical interface
- 4 LAN-WDM lanes MUX/DEMUX design
- 4x25G electrical interface
- Maximum power consumption 4W
- LC duplex connector
- Supports 103.125Gb/s bit rate
- Up to 10km transmission on single mode fiber
- Commercial case temperature range of 0°C to 70°C
- Single 3.3V power supply
- RoHS 2.0 compliant

Application

- 100GBASE-LR4 100G Ethernet
- Telecom networking
- Data Center Interconnect
- Enterprise networking

Absolute Maximum Ratings

Parameter	*Symbol*	Min.	Typ.	Max.	Units	Note
Storage Temperature	*Ts*	-40		85	°C	
Maximum Supply Voltage	*Vcc*	-0.5	3.3	3.6	V	
Relative Humidity	*RH*	5		85	%	1
Damaged Threshold, each Lane	*THd*	5.5			dBm	

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	Ts	-40	85	℃	
Power Supply Voltage	Vcc	-0.5	3.6	V	
Relative Humidity(non-condensation)	RH	0	85	%	

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Damage Threshold, each Lane	THd	5.5		dBm	
Operating Case Temperature	T_{op}	0	70	℃	

Diagnostics Monitoring

Performance Item	*Related Bytes(A0[00] memory)*	Monitor Error	Notes
Module temperature	*22 to 23*	+/-3°C	1, 2
Module voltage	*26 to 27*	< 3%	2
LD Bias current	*42 to 49*	< 10%	2
Transmitter optical power	*50 to 57*	< 3dB	2
Receiver optical power	*34 to 41*	< 3dB	2

Optical Characteristics

Parameter	*Symbol*	Min.	*Typ.*	Max.	*Units Note*	Notes
Transmit wavelengths		*1294.53*		*1296.59*	*nm*	
		1299.02		*1301.09*	*nm*	
		1303.54		*1305.63*	*nm*	
		1308.09		*1310.19*	*nm*	
Transmitter						
Signaling Speed per Lane	*25.78125± 100 ppm*				*Gb/s*	
Side-mode Suppression Ratio (SMSR)	*SMSR*	30			*dB*	
Total Average Launch Power				10.5	*dBm*	
Average launch power, each Lane	*PAVG*	-4.3		4.5	*dBm*	
Optical Modulation Amplitude (OMA),each Lane	*POMA*	-1.3		4.5	*dBm*	
Transmitter and Dispersion Penalty (TDP), each lane				2.2	dB	
Extinction Ratio(ER)	*ER*	4			*dB*	
Launch power in OMA minus TDP, each lane		-2.3			*dBm*	
Transmitter Reflectance	*Rt*			-12	*dB*	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}	{0.25, 0.4, 0.45, 0.25, 0.28, 0.4}					1
Receiver						
Receive wavelengths		1294.53		1296.59	nm	
		1299.02		1301.09	nm	

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		1303.54		1305.63	nm	
		1308.09		1310.19	nm	
Signaling Speed per Lane		25.78125± 100 ppm			Gb/s	
Average Receiver Power, each Lane		-10.6		4.5	dBm	
Receiver power, each lane (OMA)				4.5	dBm	
Channel power difference				5.5	dB	
Damage threshold, each lane		5.5			dBm	
Receiver sensitivity (OMA), each lane				-8.6	dBm	2
Stressed receiver Sensitivity (OMA), each lane				-6.8	dBm	2
LOS Assert		-26			dBm	
LOS Deassert				-13	dBm	
LOS Hysteresis		0.5			dB	
Receiver reflectance				-26	dB	
Vertical eye closure penalty, each lane			1.8		dB	
Stressed eye J2 Jitter, each lane			0.3		UI	
Stressed eye J9 Jitter, each lane			0.47		UI	

Parameter	Symbol	Min.	Typ.	Max.	Units	Note
Power Consumption				4	W	
Supply Current	Icc			1.1544	A	Steady state
Transmitter (each Lane)						
Data Rate, each Lane	25.78125				Gbps	
Differential Input Voltage swing	Vin, pp			900	mV	At 1 MHz
Transition time	Trise/Tfall	10			ps	20%~80%
Differential Termination Re-sistance Mismatch				10	%	
Eye width	EW15	0.46			UI	
Eye height	EH15	95			mV	
Receiver (each Lane)						
Data Rate, each lane	25.78125				Gbps	
Differential output voltage swing	Vout,pp			900	mVpp	
Differential Termination Re-sistance Mismatch				10	%	At 1 MHz

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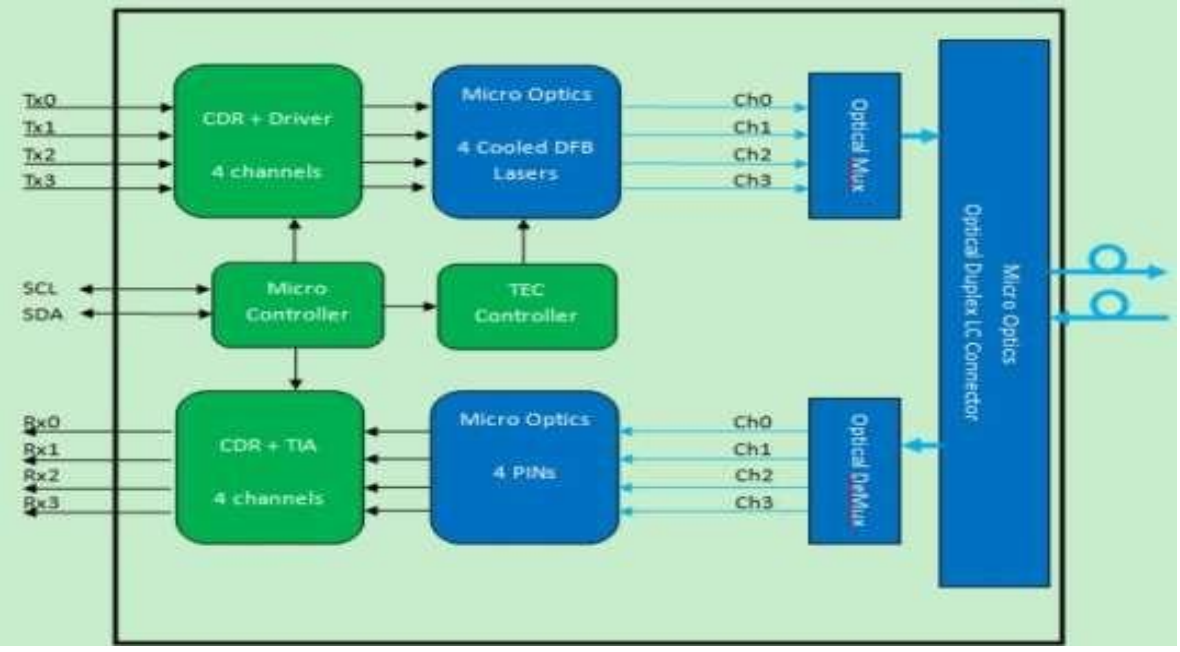
Common Mode Noise, RMS	Vrms			17.5	mV	
Transition time	Trise/Tfall	12			ps	20%~80%
Eye width	EW15	0.57			UI	
Eye height	EH15	228			mV	

Block Diagram of Transceiver



This product is a 100Gb/s transceiver module designed for optical communication applications compliant to 100GBASE-LR4 of the IEEE 802.3ba standard. The module converts 4 input channels of 25Gb/s electrical datato 4 channels of LAN WDM optical signals and then multiplexes them into a single channel for 100Gb/s optical transmission. Reversely on the receiver side, the module de-multiplexes a 100Gb/s optical input into 4 channels of LAN WDM optical signals and then converts them to 4 output channels of electrical data.

The central wavelengths of the 4 LAN WDM channels are 1295.56, 1300.05, 1304.58 and 1309.14 nm as members of the LAN WDM wavelength grid defined in IEEE 802.3ba. The high-performance cooled LAN WDMDFB transmitters and high sensitivity PIN receivers provide superior performance for 100Gigabit Ethernet applications up to 10km links and compliant to optical interface with 100GBASE-LR4 requirements specified inIEEE 802.3ba Clause 88.

The product is designed with form factor, optical/electrical connection and digital diagnostic interface accordingto the QSFP+ Multi-Source Agreement (MSA). It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

The transceiver module receives 4 channels of 25Gb/s electrical data, which are processed by a 4-channel Clock and Data Recovery (CDR) IC that reshapes and reduces the jitter of each electrical signal. Subsequently,DFB laser driver IC converts each one of the 4 channels of electrical signals to an optical signal that is transmitted from one of the 4 cooled DFB lasers which are packaged in the Transmitter Optical Sub-Assembly (TOSA). Each laser launches the optical signal in specific wavelength specified in IEEE 802.3ba 100GBASE- LR4 requirements. These 4-lane optical signals will be optically multiplexed into a single fiber by a 4-to-1 opticalWDM MUX. The optical output power of each channel is maintained constant by an automatic power control (APC) circuit. The transmitter output can be turned off by TX_DIS hardware

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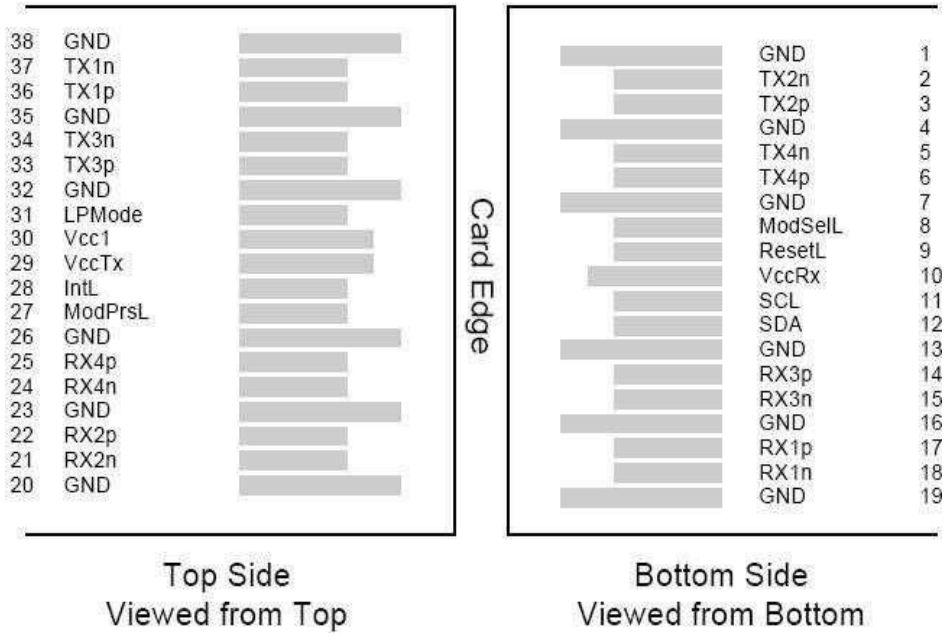
signal and/or 2-wire serial interface.

The receiver receives 4-lane LAN WDM optical signals. The optical signals are de-multiplexed by a 1-to-4 optical DEMUX and each of the resulting 4 channels of optical signals is fed into one of the 4 receivers that are packaged into the Receiver Optical Sub-Assembly (ROSA). Each receiver converts the optical signal to an electrical signal. The regenerated electrical signals are retimed and de-jittered and amplified by the RX portion of the 4-channel CDR. The retimed 4-lane output electrical signals are compliant with IEEE CAUI-4 interface requirements. In addition, each received optical signal is monitored by the DOM section. The monitored value isreported through the 2-wire serial interface. If one or more received optical signal is weaker than the threshold level, RX_LOS hardware alarm will be triggered.

A single +3.3V power supply is required to power up this product. Both power supply pins VccTx and VccRx are internally connected and should be applied concurrently. As per MSA specifications, the module offers 7 low speed hardware control pins (including the 2-wire serial interface): ModSelL, SCL, SDA, ResetL, LPMode, ModPrsL and IntL. Module Select (ModSelL) is an input pin. When held low by the host, this product responds to 2-wire serial communication commands. The ModSelL allows the use of this product on a single 2-wire interface bus – individual ModSelL lines must be used. Serial Clock (SCL) and Serial Data (SDA) are required for the 2-wire serial bus communication interface and enable the host to access the QSFP28 memory map.
The ResetL pin enables a complete reset, returning the settings to their default state, when a low level on the ResetL pin is held for longer than the minimum pulse length. During the execution of a reset the host shall disregard all status bits until it indicates a completion of the reset interrupt. The product indicates this by posting an IntL (Interrupt) signal with the Data_Not_Ready bit negated in the memory map. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset. Low Power Mode (LPMode) pin is used to set the maximum power consumption for the product in order to protect hosts that are not capable of cooling higher power modules, should such modules be accidentally inserted. Module Present (ModPrsL) is a signal local to the host board which, in the absence of a product, is normally pulled up to the host Vcc. When the product is inserted into the connector, it completes the path to ground through a resistor on the host board and asserts the signal. ModPrsL then indicates its present by setting ModPrsL to a “Low” state. Interrupt (IntL) is an output pin. “Low” indicates a possible operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and must be pulled to the Host Vcc voltage on the Host board.

Pin Assignment (MSA compliant connector)



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Pin Descriptions

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3V Power supply transmitter	
30	Vcc1	+3.3V Power supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1

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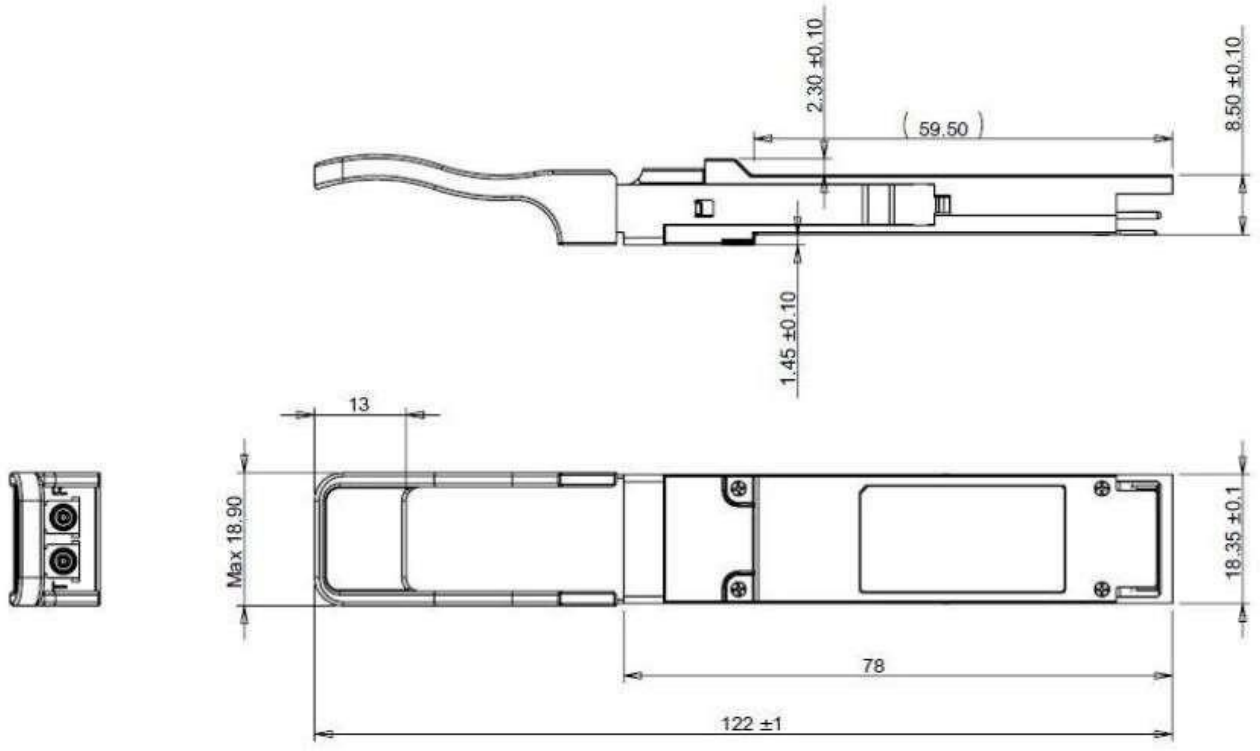
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Note:

1. GND is the symbol for signal and supply (power) common for the QSFP28 module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal common ground plane.
2. VccRx, Vcc1 and VccTx are the receiving and transmission power suppliers and shall be applied concurrently. Recommended host board power supply filtering is shown in Figure 3 below. Vcc Rx, Vcc1 andVcc Tx may be internally connected within the module in any combination. The connector pins are each ratedfor a maximum current of 1000mA.

Dimensions



Note: Dimensions are in mm, All Dimensions are 0.2mm unless otherwise specified

Ordering information:

Model Number	Part Number	Voltage	Temperature
100G QSFP28 LR4	OPCW-S10-13-CR	3.3V	0°C to 70 °C

Note: All information contained in this document is subject to change without notice.

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